REMARKS

This Amendment is in response to the Office Action mailed on November 20, 2002.

Claims 1 through 75 are currently pending in the application.

Applicants have amended claims 1, 23, 33, and 45 and, in view of the amendments and remarks submitted herein, respectfully request reconsideration of the above-referenced application.

Preliminary Amendment

Applicants' undersigned attorney notes the filing herein of a Preliminary Amendment on September 24, 2001, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, Applicants' undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

35 U.S.C. § 103(a) Obviousness Rejections

Claims 1 through 6, 10 through 17, 21 through 27, 31 through 37, 41 through 49, 51 through 55, 57 through 64, and 66 through 73 were rejected under 35 U.S.C. §103(a) as being unpatentable over Satoh (U.S. Patent 6,338,980, hereinafter "Satoh").

Claims 7 through 9, 18 through 20, 28 through 30, 38 through 40, 50, 56, 65, 74, and 75 were rejected under 35 U.S.C. §103(a) as being unpatentable over Satoh as applied above, and further in view of the admitted prior art.

Claims 1 through 75 were rejected under 35 U.S.C. §103(a) as being obvious over Grigg et al. (US 2002/0068453, hereinafter "Grigg").

Applicants submit that in order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed

combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Satoh discloses a method for manufacturing a semiconductor device and an IC chip which can meet demand of small-sizing and thinning. More particularly, the invention relates to a method for manufacturing a chip-scale package and an IC chip, which can manufacture a thin chip-scale package by back grinding in a state where an active face of an IC wafer is protected (Satoh, col. 1, lines 6-13). Satoh's method includes: a semiconductor device forming step of forming a plurality of pad in predetermined positions on an active face of the IC wafer; an electrode forming step of forming a projected electrode in a pad formed on an active face of an IC wafer; a groove forming step of forming a groove in the active face of the IC wafer along a line that the IC wafer is divided into individual pieces; a protective resin applying step of applying a protective resin on the active face of the IC wafer including the groove; an adhesive member applying step of applying an adhesive member on the active face on which the protective resin is applied; a grinding step of grinding an inactive face of the IC wafer which is fixed by the adhesive member until the groove is reached to the inactive face of the IC wafer; an adhesive member removing step of removing the adhesive member applied to the active face; and a separating step of applying an adhesive member to the ground face of the IC wafer, which has been ground in the grinding step, dicing the protective resin along the lines into chip-scale packages in a state where the IC wafer is fixed by the adhesive member and, after that, removing the adhesive member applied to the ground face (*Id.*, col. 3, lines 28-51).

The Office Action acknowledges that Satoh does not disclose an adhesive member having a backing (Office Action, item 2, second paragraph), thinning through chemical-mechanical polishing (*Id.*, fourth paragraph), and the thickness of the wafer pre and post thinning (*Id.*, item 3, first paragraph). In addition, Applicants point out that the following elements not taught nor suggested by the cited prior art reference. Satoh does not teach nor suggest (1) attaching an adhesive tape having a backing on only a portion of the active surface of a wafer; (2) applying adhesive to a portion of the surface of wafer and attaching a backing to at least a portion of the adhesive; (3) applying an adhesive with a backing to at least a portion of the bumps on the active

surface of the wafer; and (4) attaching an adhesive tape having a backing for adhesively attaching a portion of the surface of wafer to a mount assembly.

Applicants respectfully submit that Satoh cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C § 103 regarding the invention recited in independent claims 1, 12, 23, 33, 45, 51, 57, and 67 because the reference does not teach or suggest all of the claim limitations recited therein.

As to presently amended claim 1, among other recited elements, Satoh does not teach nor disclose the limitation of "attaching a tape having an adhesive and a backing on a portion of said surface of said wafer suction surface." This is so because of the fact that Satoh only discloses placing an adhesive layer without a backing to the entire surface of the wafer.

As to claim 12, among other recited elements, Satoh does not teach nor disclose the limitation of "applying an adhesive to a portion of said surface of said wafer; and attaching a backing to at least a portion of said adhesive." Satoh does not teach nor suggest these recited limitations of claim 12 because Satoh only discloses placing an adhesive layer without a backing to the entire surface of the wafer. In addition, Applicants respectfully submit that the Office's characterization of the elements recited in claim 12 uses impermissible hindsight to trivialize the invention. The Office Action states that "when providing a backing to an adhesive member that either the adhesive is applied to the object first and then the backing is applied or the adhesive is applied to the backing and then the adhesive is applied to the object. It would have been obvious to one of ordinary skill in the art to provide the adhesive to the active surface of the wafer and then applying the backing in the method of Satoh" (Office Action, item 2, fourth paragraph). Such an incorrect analysis does not consider (1) the recited limitation of attaching the backing only to a portion of the adhesive, and (2) the fact that applying the backing material by the method of Satoh, which method does not teach the use of a backing material, can only be justified by either the impermissible use of (*i*) hindsight or (*ii*) the knowledge available in the prior art to provide such a suggestion.

As to presently amended claim 23, Satoh does not teach or suggest a method "providing a wafer having bumps on at least a portion of a surface thereof; attaching an adhesive having a backing to a portion of said at least a portion of said surface of said wafer."

As to presently amended claim 33, Satoh does not teach nor suggest the claim limitation of "applying an adhesive having a backing on to a portion of said bumps of said front surface of said wafer." This is so because Satoh only discloses and teaches the use of an adhesive without backing to the bumps on the active surface of a wafer. Satoh does not teach nor suggest these recited limitations of claim 23 because Satoh only discloses placing an adhesive layer without a backing to the entire surface of the wafer.

As to presently amended claim 45, Satoh does not teach nor suggest the limitation of "applying an adhesive having a backing to a portion of said bumps and at least a portion of said surface of said wafer." Again, this is so because Satoh only discloses and teaches the use of an adhesive without backing to the bumps on the active surface of a wafer.

As to claim 51, Satoh does not teach nor suggest the limitation of "applying an adhesive having a backing to at least a portion of said front surface of said wafer covering at least one bump of said bumps thereon." Satoh only describes the use of an adhesive without a backing over all the bumps in an active surface of a wafer.

As far as claim 57 is concerned, Satoh does not teach nor suggest a wafer mount assembly comprising the limitation of "an adhesive tape having an adhesive and a backing, said adhesive tape for adhesively attaching a portion of said front surface of said wafer having said at least one bump thereon to a portion of said wafer mount assembly." Satoh only teaches or describes the use of an adhesive without a backing to hold or attach the active surface of a wafer to a wafer mount.

Finally, as to claim 67, Applicants respectfully submit that Satoh does not teach nor suggest the claim limitation of "a tape having an adhesive and a backing, said tape for adhesively attaching a portion of said wafer having said at least one bump thereon." Satoh only describes the use of an adhesive without a backing to attach the wafer to the wafer mount.

In addition, claims 2 through 6, 10 and 11, claims 13 through 17, 21, and 22, claims 24 through 27, 31, and 32, claims 34 through 37, and 41 through 44, claims 46 through 49, claims 52 through 55, claims 58 through 64, and 66, and claims 68 through 73 are each allowable, among other reasons, as depending either directly or indirectly from claims 1, 12, 23, 33, 45, 51, 57, and 67, respectively, which are allowable.

Tuning the attention now to the rejection of claims 7 through 9, 18 through 20, 28 through 30, 38 through 40, 50, 56, 65, 74, and 75 under 35 U.S.C. §103(a) as being unpatentable over Satoh as applied to claims 1 through 6, 10 through 17, 21 through 27, 31 through -37, 41 through 49, 51 through 55, 57 through 64, and 66 through 73, and further in view of the admitted prior art, Applicants respectfully submit that the combination cannot make the rejected claims obvious because it does not disclose or teach all of the recited limitations. As discussed above, Satoh does not and cannot establish a *prima facie* case of obvious under 35 U.S.C. § 103 regarding any of the independent claims of the present invention. In addition, the admitted prior art does not disclose the elements not taught nor suggested by Satoh in order to correct the shortcomings thereof. Therefore, the combination of Satoh and the admitted prior art cannot and does not establish a *prima facie* case of obvious under 35 U.S.C. § 103 regarding any of the inventions recited in the independent claims of the above-referenced application. Thus, claims 7 through 9, 18 through 20, 28 through 30, 38 through 40, 50, 56, 65, 74, and 75 are allowable since they dependent from claims that are allowed.

Finally, claims 1 through 75 were rejected under 35 U.S.C. §103(a) as being obvious over Grigg. Applicants respectfully submit that, under 35 U.S.C. § 103(c), the obviousness rejections based on Grigg can be overcome by the provisions of 35 U.S.C. § 103(c), which provides:

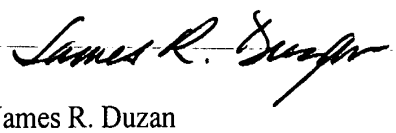
> "Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person."

The above-referenced application, which is owned by Micron Technology, Inc., as indicated by the Assignment recorded by the Patent Office on May 14, 2001, at reel/frame: 011808/0143, has an effective filing date of May 14, 2001. Grigg, which was filed on December 6, 2000, but did not publish as a patent application publication until June 6, 2002, only qualifies as prior art under 35 U.S.C. § 102(e) and is also assigned to Micron Technology, Inc. as indicated by the Assignment recorded by the Patent Office on December 6, 2000, at reel/frame: 011349/0080. Thus, under the provisions of 35 U.S.C. § 103(c), Grigg cannot be used in a 35

U.S.C. § 103(a) rejection of any of the claims of the above-referenced application.

Based on the above-presented reasons, Applicants submit that claims 1 through 75 are not obvious under 35 U.S.C. §103. Therefore, Applicants respectfully request the withdrawal of these rejections and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

A marked-up version of the amended paragraph in the specification, highlighting the changes thereto, follows to clearly identify the amendments:

Please replace the Abstract paragraph on page 23 with the following:

A method and apparatus are disclosed for mounting a wafer on a [wafer] mount and thinning the wafer [on the wafer mount]. The wafer includes a front surface having bumps [located thereon] with an adhesive tape having a backing attached thereto and a back surface. [Attached to the bumps on the wafer is an adhesive tape having a backing.] [The wafer mount includes a suction surface with apertures that communicate with a vacuum.] The front surface of the wafer is mounted facedown on [the] a suction surface [with its front surface facedown] with the backing of the adhesive tape abutting the [suction] surface [of the wafer mount]. The wafer is then suctioned [to the wafer mount by the vacuum communicating with the apertures in the suction surface], after which the back surface of the wafer undergoes a grinding process to thin the wafer. Since the backing attached to the bumps on the wafer is substantially planar and sits substantially flat on the suction surface of the wafer mount, the force exerted on the wafer from the thinning process does not overcome the suction force holding the wafer on the wafer mount. Thus, the bumped wafer may be thinned without damaging the bumps and the active surface of the wafer.

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A method of attaching a wafer having bumps on a surface thereof, comprising:

attaching a tape having an adhesive and a backing on [at least] a portion of said surface of said wafer;

providing a wafer mount having a suction surface; and

applying a suction force to said backing of said tape.

23. (Twice Amended) A method of thinning a wafer comprising:

providing a wafer having bumps on at least a portion of a surface thereof;

attaching an adhesive having a backing to a portion of said at least a portion of said surface of said wafer;

providing a wafer mount having a suction surface;

attaching said backing of said adhesive to at least a portion of said suction surface of said wafer mount using a suction force; and

removing wafer material from another surface of said wafer.

33. (Twice Amended) A method of fabricating a wafer having a front surface having bumps thereon and a back surface, comprising:

applying an adhesive having a backing on to a portion of said bumps of said front surface of said wafer;

providing a wafer mount having a suction surface;

attaching at least a portion of said backing to at least a portion of said suction surface of said wafer mount using a suction force; and

removing wafer material from said back surface of said wafer.

45. (Twice Amended) A method of mounting a bumped wafer having bumps on at least a portion of a surface thereof to a wafer mounting chuck, comprising:

applying an adhesive having a backing to [at least] a portion of said bumps and at least a portion of said surface of said wafer; and

mounting said wafer to said wafer mounting chuck using a suction force communicated through said wafer mounting chuck.